

ABSTRACT OF THE DISCLOSURE

A p impurity region (3) defines a RESURF isolation region in an n⁻ semiconductor layer (2). A trench isolation structure (8a) and the p impurity region (3) together define a trench isolation region in the n⁻ semiconductor layer (2) in the RESURF isolation region. An nMOS transistor (103) is provided in the trench isolation region. A control circuit is provided in the RESURF isolation region excluding the trench isolation region. An n⁺ buried impurity region (4) is provided at the interface between the n⁻ semiconductor layer (2) and a p⁻ semiconductor substrate (1), and under an n⁺ impurity region 7 connected to a drain electrode (14) of the nMOS transistor (103).